We claim:

1. A process of operating a plurality of scan paths comprising:

A. sequentially accessing and shifting data through each one of said plurality of scan paths;

B. simultaneously accessing and loading parallel data into all of said plurality of scan paths at a first time; and

C. simultaneously accessing and loading parallel data into all of said plurality of scan paths at a second time.

2. A process of operating a plurality of scan paths comprising:

A. sequentially accessing and shifting data through each one of said plurality of scan paths; and

B. simultaneously accessing and shifting data through all of said plurality of scan paths.

3. A process of operating a plurality of scan paths comprising:

A. sequentially accessing and shifting data through each one of said plurality of scan paths;

B. simultaneously accessing and shifting data through all of said plurality of scan paths; and

C. simultaneously accessing and loading parallel data into all of said plurality of scan paths.

4. A scan path arrangement within an integrated circuit having logic circuitry to be tested, comprising:

A. a scan input terminal and a scan output terminal;

B. a scan path connected to the logic circuitry, the scan path having an input and an output;

C. a memory isolated from said logic circuitry, said memory having an input and an output;

D. a first connection formed between said scan input terminal and said memory input;

E. a second connection formed between said memory output and said scan path input; and

F. a third connection formed between said scan path output and said scan output terminal.

5. The scan path arrangement of claim 4 in which said memory and said scan path are connected to a common clocking source.